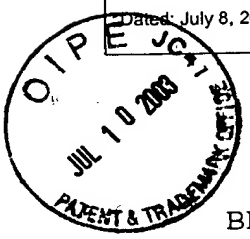
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: July 8, 2003 Signature: (Michael J. Doherty)



PATENT
TESSERA 3.0-078 DIV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of Fjelstad et al.	
Application No. 09/020,647	Group Art Unit: 2827
Filed: February 9, 1998	Examiner: D. Graybill
For: Methods of Making Compliant Semiconductor Chip Packages (As Amended)	Date: July 8, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. § 1.192(a)

Sir:

This Appeal Brief is filed pursuant to an appeal from the decision of the Primary Examiner finally rejecting the pending claims in the above-identified patent application. A petition requesting a five-month extension of time in which to file the Appeal Brief originally due February 9, 2003 is filed herewith. The Commissioner is hereby authorized to charge $1,970.00 for the five-month extension petition and the $320.00 fee for filing the Appeal Brief required by 37 C.F.R 1.17(c), and any other fees that may be due in connection with this Appeal Brief to Deposit Account No. 12-1095.

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I. REAL PARTY IN INTEREST

The real party in interest in this case is Tessera, Inc., a corporation of Delaware, having a place of business at 3099 Orchard Drive, San Jose, California 95134.

II. RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to Appellants, Appellants' attorneys or the assignee, Tessera, Inc., which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 35-57 are pending in the present application. Claims 1-34 have been cancelled. Claims 35-57 are rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

After receiving the Final Office Action mailed July 25, 2002, Applicants filed an Amendment After Final under 37 C.F.R. § 1.116 on December 3, 2002 in order to overcome a rejection under 35 U.S.C. § 112, first paragraph, and to present arguments regarding the patentability of claims 35-57. In response, the Examiner issued an Advisory Action mailed March 6, 2003. In the Advisory Action, the Examiner indicated that he entered the Amendment After Final for purposes of appeal to overcome the rejection under 35 U.S.C. § 112, first paragraph, however, the Examiner did not accept the arguments to overcome the 35 U.S.C. § 102/103 rejections. No amendments have been filed subsequent to the submission of the Amendment After Final on December 3, 2002.

V. SUMMARY OF THE INVENTION

The present invention relates to methods of making semiconductor chip packages including a semiconductor chip and a compliant layer. The invention recited in claim 35 and the other claims of the present application relates to methods of

selectively forming elongated, flexible bond ribbons over a compliant layer, whereby the elongated bond ribbons extend along sloping edges of the compliant layer. Referring to Applicants' FIGS. 1A-1E and 2, a semiconductor chip 100 has a central region 115 bounded by contacts 110 on a contact-bearing face 120 of chip 100. The contact-bearing face 120 of the chip is covered by a passivation layer 130 having apertures for exposing the chip contacts 110. Referring to FIG. 1C, a compliant layer 140 having a substantially flat top surface is formed atop passivation layer 130. The compliant layer 140 is located over the central region 115 of semiconductor chip 100 and is surrounded by the chip contacts 110. The compliant layer is formed such that it has a substantially flat top surface 147 and edges that gradually slope down to the top surface of the dielectric passivation layer 130. The sloping edges preferably have a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the compliant layer, whereby both the first transition region and the second transition region have a radius of curvature. Specification at page 5, lines 3-11.

Referring to FIG. 1D, a plating seed layer 150 is deposited atop selected portions of compliant layer 140. Referring to FIG. 1E, a photoresist 160 is applied to the exposed surfaces of the assembly and the photoresist is then exposed and developed. Elongated bond ribbons 170 are then selectively electroplated atop both the first dielectric protective layer and the compliant layer, whereby each bond ribbon electrically connects each chip contact 110 to a respective terminal 175 positioned atop the compliant layer. See Specification at page 11, lines 17-20. FIG. 2 shows a perspective view of the elongated bond ribbons extending between the chip contacts 110 and terminals 175. As clearly shown in FIG. 2, the elongated bond ribbons 170 extend along the sloping edge surfaces 145 of compliant layer 140. As noted above, the compliant layer has sloped peripheral edges so that the overlying bond ribbons are curved rather than kinked.

VII. ISSUES

Whether claims 35-38, 40-41, 45-54 and 57 are unpatentable under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 5,070,297 to *Kwon et al.* (``*Kwon*'') or, in the alternative, under 35 U.S.C. § 103(a) as obvious over the combination of *Kwon* and U.S. Patent 4,671,849 to Chen.

Whether claim 39 is unpatentable under 35 U.S.C. § 103(a) over *Kwon* or the combination of *Kwon* and *Chen* as applied to claims 35-38, 40-41, 45-54 and 57, and further in combination with U.S. Patent 4,962,985 to *LeGrange*.

Whether claim 42 is unpatentable under 35 U.S.C. § 103(a) as being unpatentable over *Kwon* or the combination of *Kwon* and *Chen* as applied to claims 35-38, 40-41, 45-54 and 57, and further in combination with U.S. Patent 5,310,699 to *Chikawa*.

Whether claims 43-44 and 55-56 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kwon* as applied to claims 35-38, 40-41, 45-54 and 57, and further in combination with U.S. Patent 5,874,782 to *Palagonia*.

VIII. GROUPING OF CLAIMS

Claims 35-38, 40-41, 45-54 and 57 stand or fall together.

Claims 43-44 and 55-56 stand or fall together.

IX. ARGUMENT

The Examiner rejected claims 35-38, 40-41, 45-54 and 57 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,070,297 to *Kwon et al.*, or in the alternative, under 35 U.S.C. § 103(a) as obvious over the combination of *Kwon* and U.S. Patent 4,671,849 to *Chen*. Referring to FIGS. 4A-4H thereof, *Kwon* discloses a method of making integrated circuit testing devices including providing a layer of a compliant material 32 atop a silicone dioxide layer 34, with active

element 36 disposed between silicone substrate 38 and silicone dioxide layer 34. Referring to FIG 4B of *Kwon*, vias are formed in compliant layers 32 to expose portions of the active element 36. Each via forms a conical-shaped opening extending between the top and bottom surfaces of compliant layer 32. Metal contact layer 28 and a conductive coating 30 are then deposited within the via openings in compliant material 32, as shown in FIG. 4C. Referring to FIG. 4D of *Kwon*, a compliant protective coating 26 is formed atop compliant material 32, metal contact layer 28 and conductive coating 30. The compliant protective coating 26 is etched to form openings extending to metal contact layer 28, and a seed layer is sputtered over the protective coating layer 26 to form a connector base in each opening in the protective coating 26. A conductive metal layer is then sputtered over connector base 24 to form connector caps 22. Referring to FIG. 4H of *Kwon*, test probes 16 are attached to the assembly and electrically interconnected with the conductive metal 28, 30 in the vias. Thus, *Kwon* teaches forming metallized vias by first forming via openings in a compliant layer and then depositing one or more layers of conductive material in the via openings.

Referring to FIG. 4B thereof, *Chen* discloses a structure including an insulating layer 10 having a curved section with a shallow slope section 20 and a steeper slope section 22.

Claim 35 patentable over *Kwon* and *Chen* because the references neither disclose nor suggest "providing a compliant layer over said dielectric protective layer..., wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to said dielectric protective layer and sloping edges between the top surface and the bottom surface, <u>wherein the sloping edges of said compliant layer have a first curved transition region near the top surface of said compliant layer and a second curved transition region near the bottom surface of said complaint layer</u>." (Emphasis added) Clearly, *Kwon's* compliant layer 32 (FIG. 2) does not have curved transition regions near the top and bottom surfaces thereof, a limitation explicitly recited in claim 35.

Claim 35 is also patentable over *Kwon* and *Chen* because the references neither disclose nor suggest "selectively electroplating elongated bond ribbons atop said dielectric protective layer and said compliant layer." The conductive metal layers 28, 30 deposited in *Kwon's* via openings do not form "elongated bond ribbons." Rather, *Kwon's* metalized vias have a "V" or conical-shaped cross section that teaches away from Applicants' claimed "elongated bond ribbons." Claim 35 is also patentable because the references neither disclose nor suggest that the "elongated bond ribbons...have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer." For all of these reasons, claim 35 is unanticipated by *Kwon*, unobvious over *Kwon* and *Chen*, and is otherwise allowable. Claims 36-38 and 40-41 are also allowable, *inter alia*, by virtue of their dependence from claim 35.

Claim 45 is patentable over *Kwon* and *Chen* because the cited references neither disclose nor suggest a method of making a compliant microelectronic package including providing a compliant layer, "wherein the sloping edges of said compliant layer have first curved transition regions near the top surface of said compliant layer and second curved transition regions near the bottom surface of said compliant layer." Claim 45 is also patentable because the cited references neither disclose nor suggest the step of "selectively forming elongated, flexible bond ribbons over the top surface and the sloping edge surfaces of said compliant layer..., wherein said elongated, flexible bond ribbons extending along the sloping edges of said compliant layer have first curved regions overlying the first curved transition regions of said compliant layer and second curved regions overlying the second curved transition regions of said compliant layer." Claims 46-54 and 57 are also patentable, *inter alia*, by virtue of their dependence either directly or indirectly from claim 45, which is patentable for the reasons set forth above.

Claim 39 is rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of *Kwon* and *Chen* and further in combination with U.S. Patent 4,962,985 to *La Grange*. Claim 39 is unobvious, *inter alia*, by virtue of its dependence from claim 35 and because *La Grange* does not overcome the deficiencies in *Kwon* and *Chen* noted above.

Claim 42 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kwon* or the combination of *Kwon* and *Chen*, and further in combination with U.S. Patent 5,310,699 to *Chikawa*. Claim 42 is unobvious, *inter alia*, by virtue of its dependence from claim 35, and because *Chikawa* does not overcome the deficiencies noted above in *Kwon* and *Chen*.

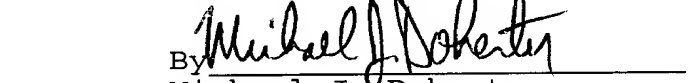
Claims 43-44 and 55-56 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kwon* in combination U.S. Patent 5,874,782 to *Palagonia*. Applicants respectfully assert that *Palagonia* does not overcome the deficiencies noted above in *Kwon*. Claims 43-44 and 55-56 are unobvious, *inter alia*, by virtue of their dependence from respective claims 35 and 45, which are unobvious for the reasons set forth above.

VIII. CONCLUSION

For the reasons set forth above, this Honorable Board should reverse the rejection as to all claims on appeal.

Dated: July 8, 2003

Respectfully submitted,

By 

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APPENDIX

A copy of the claims on appeal is set forth below:

35. A method of making a compliant semiconductor chip package comprising:

providing a semiconductor chip having a contact bearing surface including a central region bounded by a peripheral region, wherein the peripheral region of said contact bearing surface has chip contacts;

providing a dielectric protective layer over the contact bearing surface of said semiconductor chip, said dielectric protective layer having apertures for said chip contacts;

providing a compliant layer over said dielectric protective layer and over the central region of the contact bearing face of said semiconductor chip, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to said dielectric protective layer and sloping edges between the top surface and the bottom surface, wherein the sloping edges of said compliant layer have a first curved transition region near the top surface of said compliant layer and a second curved transition region near the bottom surface of said compliant layer; and

selectively electroplating elongated bond ribbons atop said dielectric protective layer and said compliant layer, wherein each said bond ribbon electrically connects one of said chip contacts to an associated conductive terminal disposed on the top surface of said compliant layer, and wherein said elongated bond ribbons extend along the sloping edges of said compliant layer and have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer.

36. The method according to Claim 35, further comprising after selectively electroplating said bond ribbons, providing a second dielectric protective layer over exposed elements on the terminal side of said package, wherein said second dielectric protective layer has a plurality of

apertures extending therethrough for providing access to said terminals.

37. The method according to Claim 35, wherein said compliant layer comprises a material selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

38. The method according to Claim 35, further including the step of providing an encapsulant layer atop an exposed surface of said bond ribbons.

39. The method according to Claim 38, wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel.

40. The method according to Claim 38, further including the step of providing a second dielectric layer atop said encapsulant layer, wherein said second dielectric layer has a plurality of apertures for providing access to said terminals.

41. The method according to Claim 35, wherein said dielectric layer is a silicon dioxide passivation layer provided on the contact bearing surface of said semiconductor chip.

42. The method according to Claim 35, further including before providing the compliant layer, plating a barrier metal atop the contacts of said semiconductor chip, wherein said barrier metal reduces voiding at an interface between the contacts and said bond ribbons.

43. The method according to Claim 35, wherein the method steps are applied simultaneously to a plurality of undiced semiconductor chips on a wafer to form a plurality of compliant semiconductor chip packages, the method further including dicing said wafer after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages.

44. The method according to Claim 35, wherein the method steps are applied simultaneously to a plurality of adjacent semiconductor chips arranged in an array to form a plurality of compliant semiconductor chip packages, the method

further including the step of dicing said adjacent packages after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages.

45. A method of making a compliant microelectronic package comprising:

providing a microelectronic element having a first surface and a plurality of contacts disposed on the first surface thereof;

providing a compliant layer over the first surface of said microelectronic element, said compliant layer having a bottom surface facing toward said first surface of said microelectronic element, a top surface facing upwardly away from said microelectronic element and one or more sloping edge surfaces extending between the top and bottom surfaces of said compliant layer, wherein the sloping edges of said compliant layer have first curved transition regions near the top surface of said compliant layer and second curved transition regions near the bottom surface of said compliant layer; and

selectively forming elongated, flexible bond ribbons over the top surface and the sloping edge surfaces of said compliant layer for electrically connecting said contacts to conductive terminals overlying the top surface of said compliant layer, wherein said elongated, flexible bond ribbons extending along the sloping edges of said compliant layer have first curved regions overlying the first curved transition regions of said compliant layer and second curved regions overlying the second curved transition regions of said compliant layer.

46. The method as claimed in claim 45, wherein the contacts are disposed in a first region of the first surface of said microelectronic element, and said compliant layer overlies a second region of the first surface of said microelectronic element, and wherein the sloping edges of said compliant layer extend along one or more borders between the first and second regions of the first surface of said microelectronic element.

47. The method as claimed in claim 45, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons.

48. The method as claimed in claim 45, wherein said selectively forming bond ribbons step includes depositing a conductive material over the top of said package and etching away portions of said conductive material.

49. The method as claimed in claim 45, further comprising:

before the providing a compliant layer step, providing a first dielectric protective layer over the first surface of said microelectronic element, the first dielectric layer having a plurality of apertures in substantial alignment with said contacts for providing access to said contacts, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer.

50. The method as claimed in claim 49, the selectively forming flexible bond ribbons step including electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer.

51. The method as claimed in claim 45, further including the step of providing a dielectric cover layer over said compliant layer and said bond ribbons after the step of selectively forming said bond ribbons, wherein said dielectric cover layer has a plurality of apertures for accessing said terminals therethrough.

52. The method as claimed in claim 45, further including the step of providing an encapsulant layer over an exposed surface of said bond ribbons.

53. The method as claimed in claim 52, further including the step of providing a second dielectric protective layer atop the encapsulant layer, wherein the second dielectric protective layer has a plurality of apertures for accessing said terminals therethrough.

54. The method as claimed in claim 45, further including before the step of forming said bond ribbons, depositing a barrier metal atop said contacts, wherein said

barrier metal minimizes voiding between said contacts and said bond ribbons.

55. The method as claimed in claim 45, wherein the method is applied to a plurality of undiced semiconductor chips on a wafer to form a plurality of compliant semiconductor chip packages, the method further comprising separating said packages after the selectively forming elongated, flexible bonds ribbons step.

56. The method as claimed in claim 45, wherein the method is applied to a plurality of adjacent semiconductor chips arranged in an array to form a corresponding plurality of compliant semiconductor chip packages, the method further comprising separating the plurality of compliant semiconductor chip packages from one another following the step of selectively electroplating said bond ribbons.

57. The method as claimed in claim 45, wherein the sloping edge surfaces of said compliant layer extend in both vertical and horizontal directions.

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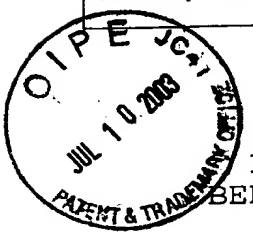

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APPEAL BRIEF UNDER 37 C.F.R. § 1.192(a)

Sir:

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V. SUMMARY OF THE INVENTION

The present invention relates to methods of making semiconductor chip packages including a semiconductor chip and a compliant layer. The invention recited in claim 35 and the other claims of the present application relates to methods of

selectively forming elongated, flexible bond ribbons over a compliant layer, whereby the elongated bond ribbons extend along sloping edges of the compliant layer. Referring to Applicants' FIGS. 1A-1E and 2, a semiconductor chip 100 has a central region 115 bounded by contacts 110 on a contact-bearing face 120 of chip 100. The contact-bearing face 120 of the chip is covered by a passivation layer 130 having apertures for exposing the chip contacts 110. Referring to FIG. 1C, a compliant layer 140 having a substantially flat top surface is formed atop passivation layer 130. The compliant layer 140 is located over the central region 115 of semiconductor chip 100 and is surrounded by the chip contacts 110. The compliant layer is formed such that it has a substantially flat top surface 147 and edges that gradually slope down to the top surface of the dielectric passivation layer 130. The sloping edges preferably have a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the compliant layer, whereby both the first transition region and the second transition region have a radius of curvature. Specification at page 5, lines 3-11.

Referring to FIG. 1D, a plating seed layer 150 is deposited atop selected portions of compliant layer 140. Referring to FIG. 1E, a photoresist 160 is applied to the exposed surfaces of the assembly and the photoresist is then exposed and developed. Elongated bond ribbons 170 are then selectively electroplated atop both the first dielectric protective layer and the compliant layer, whereby each bond ribbon electrically connects each chip contact 110 to a respective terminal 175 positioned atop the compliant layer. See Specification at page 11, lines 17-20. FIG. 2 shows a perspective view of the elongated bond ribbons extending between the chip contacts 110 and terminals 175. As clearly shown in FIG. 2, the elongated bond ribbons 170 extend along the sloping edge surfaces 145 of compliant layer 140. As noted above, the compliant layer has sloped peripheral edges so that the overlying bond ribbons are curved rather than kinked.

VII. ISSUES

Whether claims 35-38, 40-41, 45-54 and 57 are unpatentable under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 5,070,297 to *Kwon et al.* (``*Kwon*'') or, in the alternative, under 35 U.S.C. § 103(a) as obvious over the combination of *Kwon* and U.S. Patent 4,671,849 to Chen.

Whether claim 39 is unpatentable under 35 U.S.C. § 103(a) over *Kwon* or the combination of *Kwon* and *Chen* as applied to claims 35-38, 40-41, 45-54 and 57, and further in combination with U.S. Patent 4,962,985 to *LeGrange*.

Whether claim 42 is unpatentable under 35 U.S.C. § 103(a) as being unpatentable over *Kwon* or the combination of *Kwon* and *Chen* as applied to claims 35-38, 40-41, 45-54 and 57, and further in combination with U.S. Patent 5,310,699 to *Chikawa*.

Whether claims 43-44 and 55-56 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kwon* as applied to claims 35-38, 40-41, 45-54 and 57, and further in combination with U.S. Patent 5,874,782 to *Palagonia*.

VIII. GROUPING OF CLAIMS

Claims 35-38, 40-41, 45-54 and 57 stand or fall together.

Claims 43-44 and 55-56 stand or fall together.

IX. ARGUMENT

The Examiner rejected claims 35-38, 40-41, 45-54 and 57 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,070,297 to *Kwon et al.*, or in the alternative, under 35 U.S.C. § 103(a) as obvious over the combination of *Kwon* and U.S. Patent 4,671,849 to *Chen*. Referring to FIGS. 4A-4H thereof, *Kwon* discloses a method of making integrated circuit testing devices including providing a layer of a compliant material 32 atop a silicone dioxide layer 34, with active

element 36 disposed between silicone substrate 38 and silicone dioxide layer 34. Referring to FIG 4B of *Kwon*, vias are formed in compliant layers 32 to expose portions of the active element 36. Each via forms a conical-shaped opening extending between the top and bottom surfaces of compliant layer 32. Metal contact layer 28 and a conductive coating 30 are then deposited within the via openings in compliant material 32, as shown in FIG. 4C. Referring to FIG. 4D of *Kwon*, a compliant protective coating 26 is formed atop compliant material 32, metal contact layer 28 and conductive coating 30. The compliant protective coating 26 is etched to form openings extending to metal contact layer 28, and a seed layer is sputtered over the protective coating layer 26 to form a connector base in each opening in the protective coating 26. A conductive metal layer is then sputtered over connector base 24 to form connector caps 22. Referring to FIG. 4H of *Kwon*, test probes 16 are attached to the assembly and electrically interconnected with the conductive metal 28, 30 in the vias. Thus, *Kwon* teaches forming metallized vias by first forming via openings in a compliant layer and then depositing one or more layers of conductive material in the via openings.

Referring to FIG. 4B thereof, *Chen* discloses a structure including an insulating layer 10 having a curved section with a shallow slope section 20 and a steeper slope section 22.

Claim 35 patentable over *Kwon* and *Chen* because the references neither disclose nor suggest "providing a compliant layer over said dielectric protective layer..., wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to said dielectric protective layer and sloping edges between the top surface and the bottom surface, wherein the sloping edges of said compliant layer have a first curved transition region near the top surface of said compliant layer and a second curved transition region near the bottom surface of said complaint layer." (Emphasis added) Clearly, *Kwon's* compliant layer 32 (FIG. 2) does not have curved transition regions near the top and bottom surfaces thereof, a limitation explicitly recited in claim 35.

Claim 35 is also patentable over *Kwon* and *Chen* because the references neither disclose nor suggest "selectively electroplating elongated bond ribbons atop said dielectric protective layer and said compliant layer." The conductive metal layers 28, 30 deposited in *Kwon's* via openings do not form "elongated bond ribbons." Rather, *Kwon's* metalized vias have a "V" or conical-shaped cross section that teaches away from Applicants' claimed "elongated bond ribbons." Claim 35 is also patentable because the references neither disclose nor suggest that the "elongated bond ribbons...have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer." For all of these reasons, claim 35 is unanticipated by *Kwon*, unobvious over *Kwon* and *Chen*, and is otherwise allowable. Claims 36-38 and 40-41 are also allowable, *inter alia*, by virtue of their dependence from claim 35.

Claim 45 is patentable over *Kwon* and *Chen* because the cited references neither disclose nor suggest a method of making a compliant microelectronic package including providing a compliant layer, "wherein the sloping edges of said compliant layer have first curved transition regions near the top surface of said compliant layer and second curved transition regions near the bottom surface of said compliant layer." Claim 45 is also patentable because the cited references neither disclose nor suggest the step of "selectively forming elongated, flexible bond ribbons over the top surface and the sloping edge surfaces of said compliant layer..., wherein said elongated, flexible bond ribbons extending along the sloping edges of said compliant layer have first curved regions overlying the first curved transition regions of said compliant layer and second curved regions overlying the second curved transition regions of said compliant layer." Claims 46-54 and 57 are also patentable, *inter alia*, by virtue of their dependence either directly or indirectly from claim 45, which is patentable for the reasons set forth above.

Claim 39 is rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of *Kwon* and *Chen* and further in combination with U.S. Patent 4,962,985 to *La Grange*. Claim 39 is unobvious, *inter alia*, by virtue of its dependence from claim 35 and because *La Grange* does not overcome the deficiencies in *Kwon* and *Chen* noted above.

Claim 42 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kwon* or the combination of *Kwon* and *Chen*, and further in combination with U.S. Patent 5,310,699 to *Chikawa*. Claim 42 is unobvious, *inter alia*, by virtue of its dependence from claim 35, and because *Chikawa* does not overcome the deficiencies noted above in *Kwon* and *Chen*.

Claims 43-44 and 55-56 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kwon* in combination U.S. Patent 5,874,782 to *Palagonia*. Applicants respectfully assert that *Palagonia* does not overcome the deficiencies noted above in *Kwon*. Claims 43-44 and 55-56 are unobvious, *inter alia*, by virtue of their dependence from respective claims 35 and 45, which are unobvious for the reasons set forth above.

VIII. CONCLUSION

For the reasons set forth above, this Honorable Board should reverse the rejection as to all claims on appeal.

Dated: July 8, 2003

Respectfully submitted,

By 

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APPENDIX

A copy of the claims on appeal is set forth below:

35. A method of making a compliant semiconductor chip package comprising:

providing a semiconductor chip having a contact bearing surface including a central region bounded by a peripheral region, wherein the peripheral region of said contact bearing surface has chip contacts;

providing a dielectric protective layer over the contact bearing surface of said semiconductor chip, said dielectric protective layer having apertures for said chip contacts;

providing a compliant layer over said dielectric protective layer and over the central region of the contact bearing face of said semiconductor chip, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to said dielectric protective layer and sloping edges between the top surface and the bottom surface, wherein the sloping edges of said compliant layer have a first curved transition region near the top surface of said compliant layer and a second curved transition region near the bottom surface of said compliant layer; and

selectively electroplating elongated bond ribbons atop said dielectric protective layer and said compliant layer, wherein each said bond ribbon electrically connects one of said chip contacts to an associated conductive terminal disposed on the top surface of said compliant layer, and wherein said elongated bond ribbons extend along the sloping edges of said compliant layer and have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer.

36. The method according to Claim 35, further comprising after selectively electroplating said bond ribbons, providing a second dielectric protective layer over exposed elements on the terminal side of said package, wherein said second dielectric protective layer has a plurality of

apertures extending therethrough for providing access to said terminals.

37. The method according to Claim 35, wherein said compliant layer comprises a material selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

38. The method according to Claim 35, further including the step of providing an encapsulant layer atop an exposed surface of said bond ribbons.

39. The method according to Claim 38, wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel.

40. The method according to Claim 38, further including the step of providing a second dielectric layer atop said encapsulant layer, wherein said second dielectric layer has a plurality of apertures for providing access to said terminals.

41. The method according to Claim 35, wherein said dielectric layer is a silicon dioxide passivation layer provided on the contact bearing surface of said semiconductor chip.

42. The method according to Claim 35, further including before providing the compliant layer, plating a barrier metal atop the contacts of said semiconductor chip, wherein said barrier metal reduces voiding at an interface between the contacts and said bond ribbons.

43. The method according to Claim 35, wherein the method steps are applied simultaneously to a plurality of undiced semiconductor chips on a wafer to form a plurality of compliant semiconductor chip packages, the method further including dicing said wafer after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages.

44. The method according to Claim 35, wherein the method steps are applied simultaneously to a plurality of adjacent semiconductor chips arranged in an array to form a plurality of compliant semiconductor chip packages, the method

further including the step of dicing said adjacent packages after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages.

45. A method of making a compliant microelectronic package comprising:

providing a microelectronic element having a first surface and a plurality of contacts disposed on the first surface thereof;

providing a compliant layer over the first surface of said microelectronic element, said compliant layer having a bottom surface facing toward said first surface of said microelectronic element, a top surface facing upwardly away from said microelectronic element and one or more sloping edge surfaces extending between the top and bottom surfaces of said compliant layer, wherein the sloping edges of said compliant layer have first curved transition regions near the top surface of said compliant layer and second curved transition regions near the bottom surface of said compliant layer; and

selectively forming elongated, flexible bond ribbons over the top surface and the sloping edge surfaces of said compliant layer for electrically connecting said contacts to conductive terminals overlying the top surface of said compliant layer, wherein said elongated, flexible bond ribbons extending along the sloping edges of said compliant layer have first curved regions overlying the first curved transition regions of said compliant layer and second curved regions overlying the second curved transition regions of said compliant layer.

46. The method as claimed in claim 45, wherein the contacts are disposed in a first region of the first surface of said microelectronic element, and said compliant layer overlies a second region of the first surface of said microelectronic element, and wherein the sloping edges of said compliant layer extend along one or more borders between the first and second regions of the first surface of said microelectronic element.

47. The method as claimed in claim 45, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons.

48. The method as claimed in claim 45, wherein said selectively forming bond ribbons step includes depositing a conductive material over the top of said package and etching away portions of said conductive material.

49. The method as claimed in claim 45, further comprising:

before the providing a compliant layer step, providing a first dielectric protective layer over the first surface of said microelectronic element, the first dielectric layer having a plurality of apertures in substantial alignment with said contacts for providing access to said contacts, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer.

50. The method as claimed in claim 49, the selectively forming flexible bond ribbons step including electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer.

51. The method as claimed in claim 45, further including the step of providing a dielectric cover layer over said compliant layer and said bond ribbons after the step of selectively forming said bond ribbons, wherein said dielectric cover layer has a plurality of apertures for accessing said terminals therethrough.

52. The method as claimed in claim 45, further including the step of providing an encapsulant layer over an exposed surface of said bond ribbons.

53. The method as claimed in claim 52, further including the step of providing a second dielectric protective layer atop the encapsulant layer, wherein the second dielectric protective layer has a plurality of apertures for accessing said terminals therethrough.

54. The method as claimed in claim 45, further including before the step of forming said bond ribbons, depositing a barrier metal atop said contacts, wherein said

barrier metal minimizes voiding between said contacts and said bond ribbons.

55. The method as claimed in claim 45, wherein the method is applied to a plurality of undiced semiconductor chips on a wafer to form a plurality of compliant semiconductor chip packages, the method further comprising separating said packages after the selectively forming elongated, flexible bonds ribbons step.

56. The method as claimed in claim 45, wherein the method is applied to a plurality of adjacent semiconductor chips arranged in an array to form a corresponding plurality of compliant semiconductor chip packages, the method further comprising separating the plurality of compliant semiconductor chip packages from one another following the step of selectively electroplating said bond ribbons.

57. The method as claimed in claim 45, wherein the sloping edge surfaces of said compliant layer extend in both vertical and horizontal directions.

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